Chapter 2

Computer Organisation

Lesson 4

Bus Structure

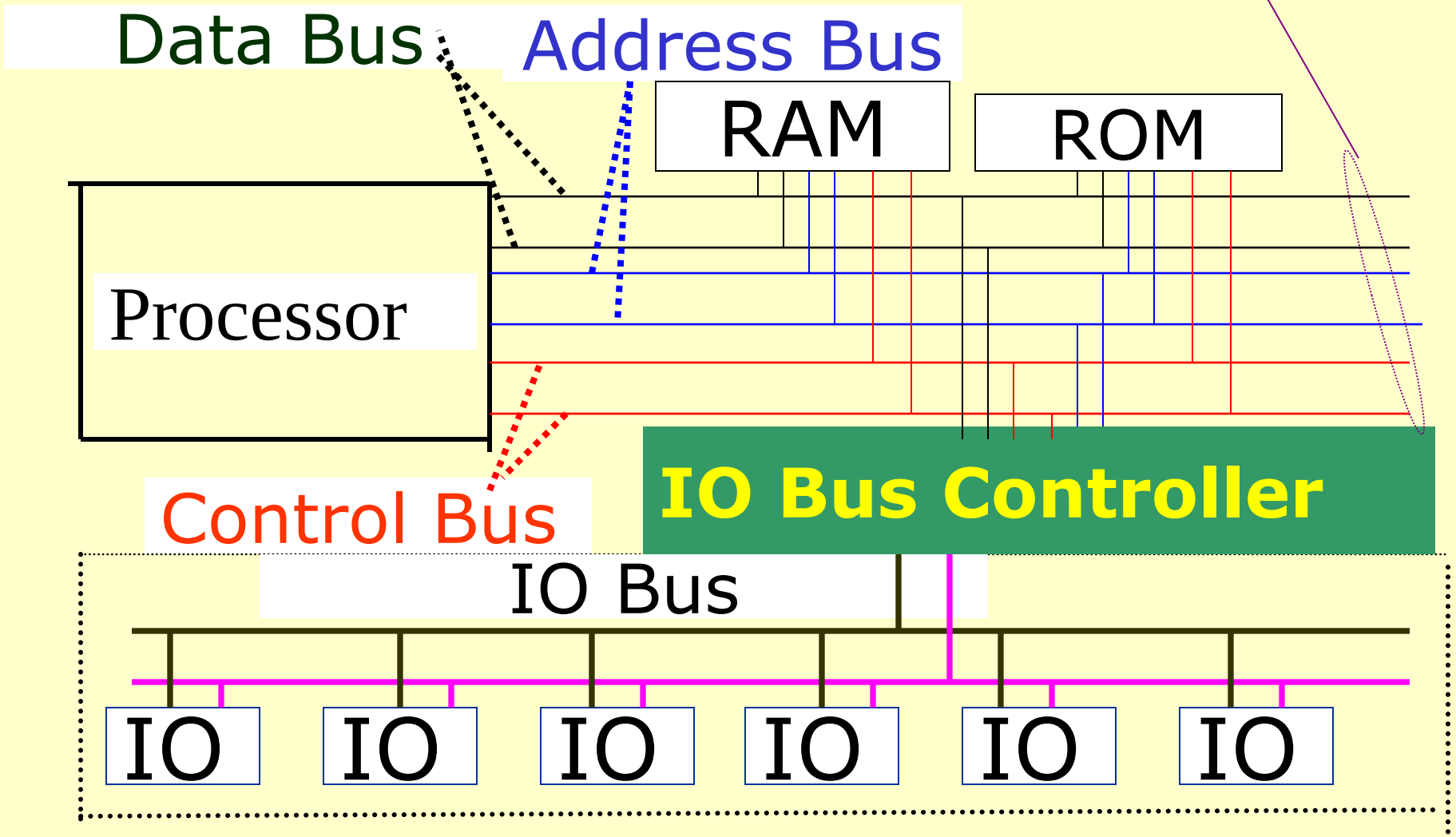
Objective —

- **Understand the functions of memory, address, control, and IO Buses**

Outline

- **Memory Bus (System Bus)**
- Address, Data and Control Buses
- IO Bus and PCI Bus

Memory (System) Bus



Memory bus

- Memory bus (also called system bus since it interconnects the subsystems)
- Interconnects the processor with the memory systems and also connects the I/O bus.
- Three sets of signals –address bus, data bus, and control bus.

System Bus

- A system's bus characteristics — according to the needs of the processor, speed, and word length for instructions and data.
- Processor internal bus(es) characteristics differ from the system external bus(es).

Outline

- Memory Bus (System Bus)
- **Address, Data and Control Buses**
- IO Bus and PCI Bus

Address Bus

1. The processor issues the address of the instruction byte or word to the memory system through the address bus.
2. The processor execution unit, when required, issues the address of the data (byte or word) to the memory system through the address bus.

32-bits **Address Bus**

- The address bus of 32-bits fetches the instruction or data from an address specified by a 32-bit number

Address Bus Example

1. Let a processor at the start reset the program counter at address 0. Then the processor issues address 0 on the bus and the instruction at address 0 is fetched from memory

Address Bus Example

2. Let a processor instruction be such that it needs to load register r1 from the memory address M. The processor issues address M on the address bus and data at address M is fetched

Data Bus

- When the Processor issues the address of the instruction, it gets back the instruction through the data bus.
- When it issues the address of the data, it loads the data through the data bus.
- When it issues the address of the data, it stores the data in the memory through the data bus.

32bit Data Bus

- A data bus of 32-bits fetches, loads, or stores the instruction or data of 32-bits.

DATA BUS USE EXAMPLE 1

- When the processor issues address *m* for an instruction, it fetches the instruction through data bus from address *m*.
- For a 32-bit instruction, word at data bus is from addresses m, m + 1, m + 2, and m + 3.

DATA BUS USE EXAMPLE 2

- When an instruction is given to store register r1 to the memory address M, the processor issues address M on the bus and sends the data at address M through the data bus. [For 32-bit data, word at data bus is to the memory addresses M, M + 1, M + 2, and M + 3.]

Control Bus

- Issues signals to control the timing of various actions during interconnection.
- Bus signals synchronize the subsystems.

Control Bus Signals

- Control signals as per the processor design.
- Signals —Address latch enable, memory ‘read’ or ‘write,’ or IO ‘read,’ or ‘write,’ or ‘data valid’, interrupt acknowledge (on a request for drawing the processor attention to an event), or hold acknowledge (on an external hold request for permitting use of the system buses)

CONTROL BUS USE EXAMPLE 1

- When the processor issues the address, it also issues a *memory-read* control signal and waits for the data or instruction.
- Memory unit must place the instruction or data during the interval in which memory-read signal is active (not inactivated by the processor).

CONTROL BUS USE EXAMPLE 2

- Let the processor issues the address on the address bus, and (after allowing sufficient time for the all address bits setup) it places the data on the data bus

CONTROL BUS USE EXAMPLE 2

- Also then issues *memory-write* control signal (after allowing sufficient time for the all data bits setup) for store signal to memory. The memory unit must write (store) the data during the interval in which memory-write signal is active (not inactivated by the processor).

Outline

- Memory Bus (System Bus)
- Address, Data and Control Buses
- **IO Bus and PCI Bus**

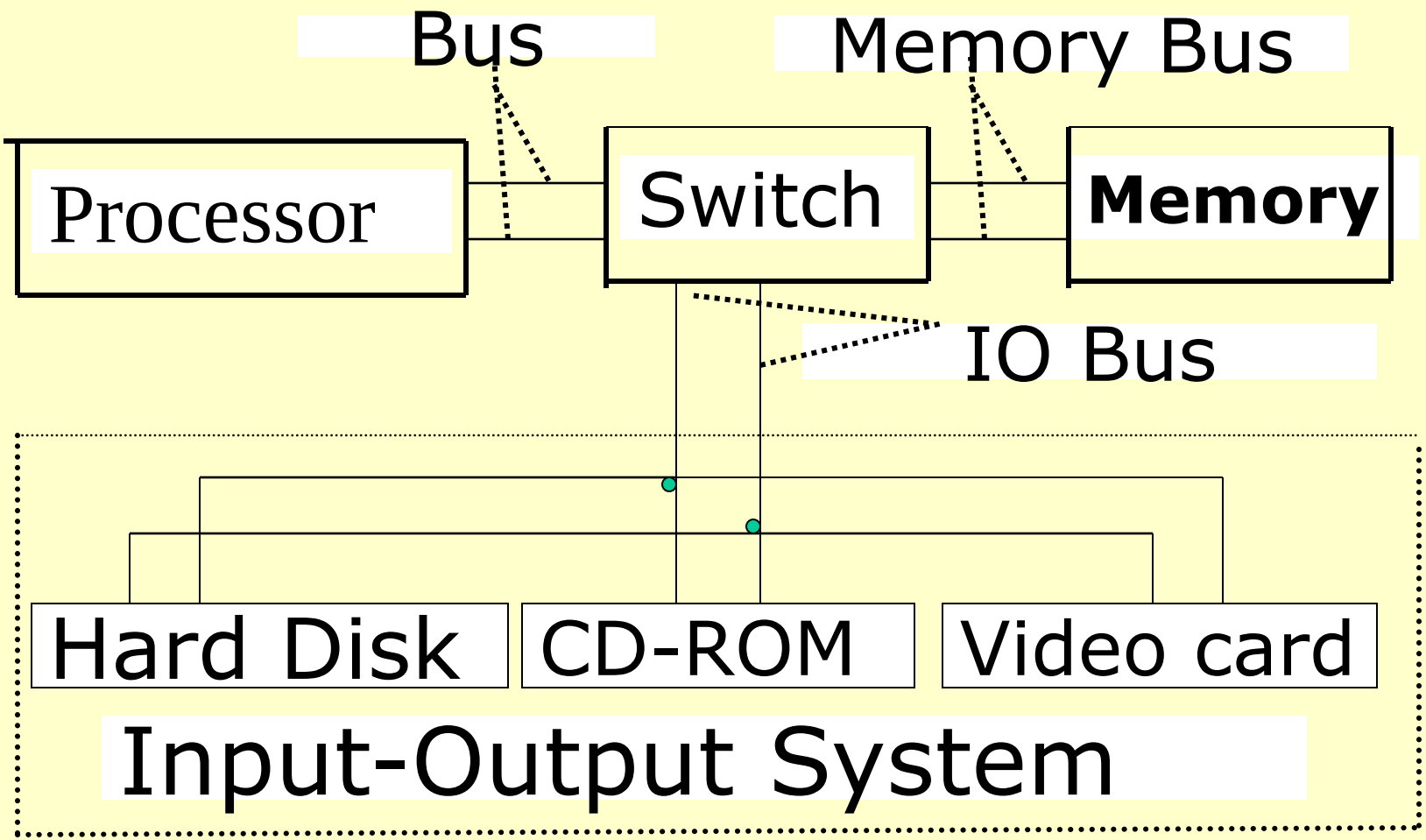
I/O Bus

- Allows a computer to interface with a wide range of I/O devices,without having to implement a specific interface for each I/O device.
- Supports a variable number of devices, allowing users to add devices to a computer after it has been purchased.

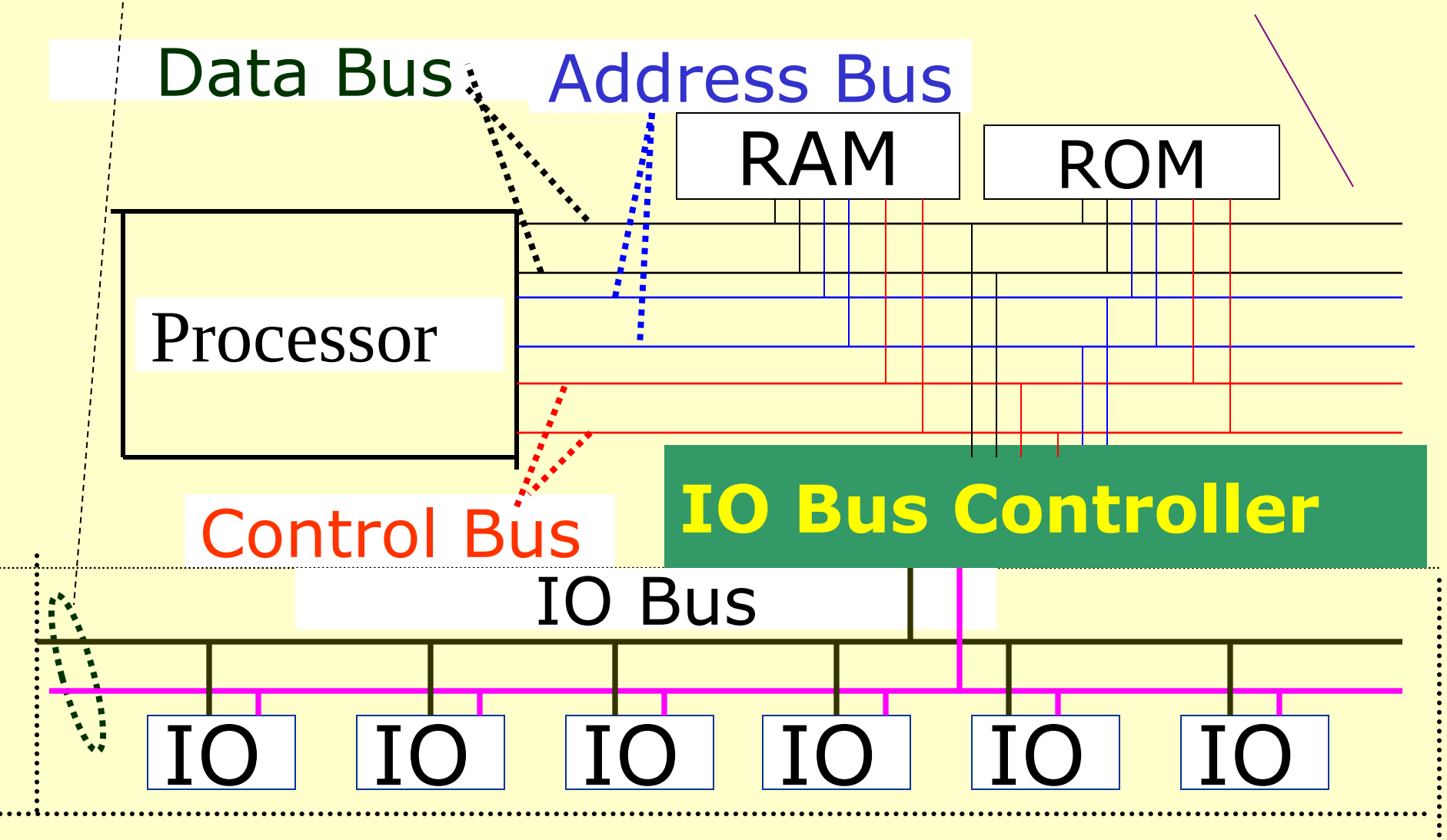
Devices on I/O Bus

- Devices can be designed to interface with the bus, allowing them to be compatible with any computer that uses the same type of I/O bus. [Chapter 11]

I/O System Switch



Devices on I/O Bus



PCI BUS

- Almost all PCs and many workstations use the PCI bus standard for their I/O bus.
- All of these systems can interface to devices designed to meet the PCI standard.
- All that is required is a *device driver* for each operating system—a program that allows the operating system to control the I/O device.

Downsides of using an I/O bus to interface to I/O devices

- All the I/O devices on a computer must share the I/O bus and I/O buses are slower than dedicated connections between the processor and an I/O device because I/O buses are designed for maximum compatibility and flexibility.

PCI bus interface

- In most systems, the processor has a single data bus that connects to a switch module such as the PCI bridge found in many PC systems

PCI bus interface

- Some processors integrate the switch module onto the same integrated circuit as the processor to reduce the number of chips required to build a system and thus the system cost.

PCI bus interface

- The switch communicates with the memory through a *memory bus*, a dedicated set of wires that transfer data between these two systems.

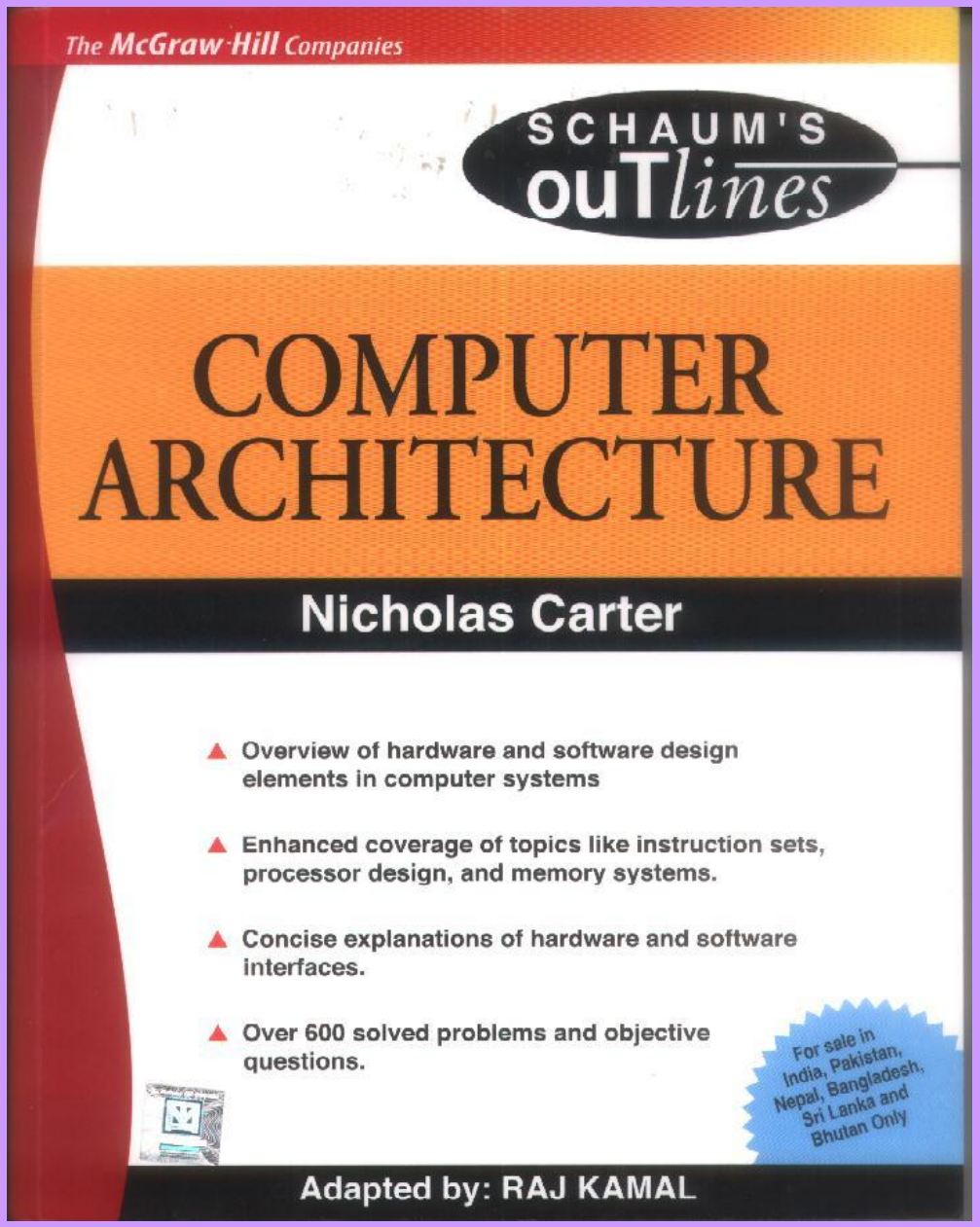
Summary

We learnt

Uses of the data, address, control and I/O Buses

End of Lesson 4 on

Bus Structure


The McGraw-Hill Companies
SCHAUM'S
ouTlines
COMPUTER
ARCHITECTURE
Nicholas Carter
Overview of hardware and software design elements in computer systems
Enhanced coverage of topics like instruction sets, processor design, and memory systems.
Concise explanations of hardware and software interfaces.
Over 600 solved problems and objective questions.
For sale in India, Pakistan, Nepal, Bangladesh, Sri Lanka and Bhutan Only
Adapted by: RAJ KAMAL

THANK YOU