## Chapter 01: Introduction

## Lesson 05: <br> Evolution of Computers Part 5- Fourth generation computers

## Objective

- Understand how electronic computers evolved during the Fourth generation of computers IBM PC and Pentium
- Greatly reduced power dissipation, space and computation time compared to $3^{\text {rd }}$ generation


## Fourth generation Electronic Systems

- 1975 onwards
- Very Large scale Transistor Integrated circuits (VLSIs) evolved for electronic circuits of microprocessors, RAMs and ROMs
- Very Very Large scale Transistor Integrated circuits (VVLSIs) evolved for electronic circuits of microprocessors, RAMs and ROMs
- Fourth generation computer systems


## VLSI s and VVLSIs

- IC with 100000-1000000 electronic logic gates a very large scale integrated (VLSI) circuit
- IC with 1000000-10000000 electronic logic gates a very large scale integrated (VVLSI) circuit


## The 4th generation Computer

- A microprocessor consisting of CPU, cache, and bus interfacing unit
- A computer consisting of the microprocessor, main memory, interrupt handler, timers, video monitor, mouse, keyboard, pen drives, hard disks, CD drives, floppy diskettes, and Ethernet card


## $4^{\text {th }}$ Generation of Computers

## Examples- <br> - IBM PC 1980 onwards <br> - Pentium 1992 onwards

## $4^{\text {th }}$ Generation Computer

- Single VLSI CPU chip as microprocessor
- Cache memory
- Large number of registers of 16- or 32-bit each with a microprocessor
- Large-sized main memory chips $(2,8,16$, or 128 MB chips) as main memory


## $4^{\text {th }}$ Generation Computer

- A large number of executable opcodes (distinct instruction)
- Addition and subtraction, multiplication and division on fixed point and floating point numbers and on multiple data types with multiple word sizes (8-bit byte, 16-bit short, 32bit word or 64-bit double word)


## $4^{\text {th }}$ Generation Computer

- The concepts of pipelining, super-scaling and multi-core execution units for execution of instructions
- Pipeline-based execution
- Processing time of the execution unit operating at faster clock rate in case of multiple instructions at the pipeline, each at a distinct logic circuit stages


## $4^{\text {th }}$ Generation Computer

- Programming in assembly and as well as in many high-level languages: for example, COBOL, PASCAL, C, C++, Java, J2EE, .net, ...
- Operating systems and software-reusable objects and modules
- 32 -bit and 64 -bit fixed as well as variable length 8 -bit to 64 -bit instruction formats


## 4th Generation Computer - Architecture



Input-Output Devices,
IO processors and the disk drive, tape drive, CD drives and line, dot, laser, inkjet printers, mouse, ...

## CPU Execution Unit

- Registers, Index Registers, Segment Registers, Flag Registers,
- Control memory (Missing in RISCs and Stack Organised Computers)
- Pipelines
- Parallel Pipelines


## CPU Registers



## IBM PC

IR, AR, SR, PC, ID, Control memory for microinstructions, 5-stage Pipeline, Dual-line for super-scaling

GPRs, Fixed Point ALU, Index and Segment registers

Input-Output Interfaces and multiple Deviceskeyboard, mouse, monitor, disk drives, COM ports and network devices (Ethernet card)

Memory (Main)
Address 0
to Address 524288
( 512 MB )

## VLSI IC reduction in circuit space requirements

- Assume- a VLSI IC needs $0.04 \times 0.03 \mathrm{~cm}^{2}$ silicon area for 1000 transistors
- There will be a reduction in circuit space requirements by a factor of $(0.4 / 0.04) \times$ $(0.3 / 0.03) \times 1000=100000$ times $=0.1$ million over a single transistor used in second generation computers


## Greatly Reduced Power Dissipation

- Assume- an IC operated at 5 V and $4 \mu \mathrm{~A}$
- Now assume a $0.13 \mu \mathrm{~m}$ VVLSI gates operate at 2 V and 10 nA
- Reduction in power dissipation by factor of $20 \mu \mathrm{~W} / 20 \mathrm{nW}=1000$ times/gate


## Greatly Enhanced Main Memory Needs

- Large programs need 512 M words, each of 32 bits
- Number of transistors required for 4 M words where each word is of 32 bits is $4 \times 4 \times 1024 \times$ $1024 \times 32=16 \mathrm{M} \times 32=512 \mathrm{M}$
- An LSI IC stores 1024 bits; therefore, the number of LSI ICs needed for 16 MB main memory will equal $512 \mathrm{M} /(1 \mathrm{~K} \times 4)=128 \mathrm{~K}$


## Greatly Reduced Memory ICs Size

- A VVLSI chip introduced in 1992 stored 16 Mbit in a single chip
- Therefore, for $16 \mathrm{MB} /(16 \mathrm{Mbit})=8$, only 8 chips were needed in 1992
- A memory stick in digital camera 8 GB in 2008


## Greatly Reduced Space

- Let an LSI IC have 1000 transistors in 0.4 cm $\times 0.4 \mathrm{~cm}$ silicon area
- Assume a $1 \mathrm{~cm}^{2}$ silicon chip has $625 \mathrm{M} / \mathrm{cm}^{2}$ number of transistors (1992)
- Assume further that a VVLSI IC has 0.04 cm $\times 0.04 \mathrm{~cm}$ area for 1 M transistors. [ $1 \mu \mathrm{~m}=1$ $\mathrm{m} / 1000000$ ]


## Greatly Reduced Space

- VVLSI IC will reduce silicon space requirement by a factor of $(1000000 / 1000) \times$ $10 \times 10=100000$ times over the third generation IC


## Greatly Reduced Space

- $0.13 \mu \mathrm{~m}$ Very-Very Large Scale Integrated Chips
- Silicon area $0.13 \mu \mathrm{~m} \times 0.13 \mu \mathrm{~m}=0.13 \times 0.13 \times$ $10^{-4} \times 10^{-4} \mathrm{~cm}^{2}=1.69 \times 10^{-10} \mathrm{~cm}^{2}$
- Density $=\left[1 /\left(1.69 \times 10^{-10}\right)\right] \mathrm{cm}^{2}=\sim 6000$ M/cm ${ }^{2}$


## Greatly Reduced Computational Time

- Assume- a transistor circuit within an LSI IC switches current from state 0 to 1 in $0.1 \mu$ s and a transistor circuit within in VLSI IC in 0.001 $\mu \mathrm{s}$
- An enhancement in processing speed by a factor of $0.1 \mu \mathrm{~s} / 0.001 \mu \mathrm{~s}, 100$ times over the speed of a third generation computer


## Greatly Reduced Computational Time

- Assume a VVLSI IC transistor switches 0 to 1 in $0.1 \mathrm{~ns}=0.0001 \mu \mathrm{~s}$
- An enhancement in processing speed by a factor of $0.1 \mu \mathrm{~s} / 0.0001 \mu \mathrm{~s}$, equal to 1000 times over the speed of a third generation computer


## Computational Performance Enhancement

## five-stage pipeline

- Improves computer performance $\sim 5$ times, as five instructions can be processed in the pipeline with execution unit operating at 5 times faster clock cycle at each instance when executing the instructions


## Computational Performance Enhancement four parallel pipelines

- Improves computer performance $\sim 4$ times, as four instructions can be processed in each pipeline with execution units in each


## Computational Performance Enhancement Multi-cores

- This improves computer performance $\sim 4$ times, as four instructions can be processed in each core with separate execution units in each


## Summary

## We learnt

- Fourth Generation computers
- VLSI and VVLSI based computers
- IBM PC and Pentiums
- Uses VLSI main RAM memories and caches
- Reduced power dissipation 1000 plus times over 3rd generation
- Reduced space 1000 times
- Reduced computational time 100 plus times
- Pipelines, parallel pipelines and multi-cores


# End of Lesson 05: <br> Evolution of Computers Part 5- Fourth generation computers 

