# Chapter 01: Introduction

## Lesson 02
## Evolution of Computers Part 2– First generation Computers

# Objective

- Understand how electronic computers evolved during the first  generation of computers
- First Generation ENIAC, EDVAC (Electronic Discrete Variable Automatic Computer) and Princeton IAS Computer

# First generation Electronic Systems

- 19th Century
- Vacuum tube valves first evolved for electronic circuits
- These tube-circuit-based computers— *first generation computers*

# 1st Generation of Computers

- 1943–1946
- ENIAC (Electronic Numerical Integrator and Calculator)
- Used ~ 18000 vacuum tubes.
- Used separate memory blocks for program and data
- Did addition, subtraction, multiplication, division, and square root
- Gave results on an electronic typewriter or punched cards

# 1st Generation of Computers 1943–1946 ENIAC

- Used 20 electronic memory units (20 accumulators)
- Used numbers that were stored as decimal digits

# 1st Generation of Computers 1943–1946 ENIAC

- Each digit had 10 valves─ off (0) or on (1)
- The 0000000001 state of the valves meant 9, 0000000010 meant 8, .., 0100000000 meant 1 and 1000 0000 00 meant 0

# 1st Generation of Computers

- 1951– EDVAC (Electronic Discrete Variable Automatic Computer)
- Used ~ 5900 vacuum tubes
- Used ‘stored programmed concept’
- Used common main memory blocks of 1024 (conventionally called 1K whenever we have to refer to a block) words

# 1st Generation Computer– 1951 EDVAC

- Fetched instructions and data into Memory blocks from a secondary memory
- The memory storage allowed the system to access data quickly for an instruction
- Used a secondary common memory of 20K words for the program (set of instructions) and data

# 1st Generation Computer– 1951 EDVAC

- Reduced the extent of hardware because data was processed serially, bit by bit, and numbers were stored as binary bits. 0000 meant 0, 0001 meant 1, .., 1001 meant 9
- Used instruction format – A1 A2 A3 A4 OP. OP was the word for defining an operation, A1 and A2 were the words for the source operand addresses, A3 was for the destination operand address and A4 was the address of next instruction

# 1st Generation Computer– 1951 EDVAC

- Used a separate instruction format for input and output operations
- Computational Speed Enhancement Over Mechanical

# IAS (Institute of Advanced Studies), Princeton computer — 1951

- Used stored programmed concept Multiple steps of Addition to arrive at the result
- Used a common main memory block of 4096 (called 4K) or 1024 (called 1K) words and 1 word = 40 bit for the fetched instructions and data

# IAS computer

- Used concept of CPU registers so data could be accessed quickly for the instruction.
- Introduced the accumulator (AC) register concept
- The AC functioned as source as well as destination operand

# IAS computer

- Had a secondary common memory of 16K words that used electromechanical devices for storing the program (set of instructions) and data
- Used a magnetic core-based memory for permanent storage of programs

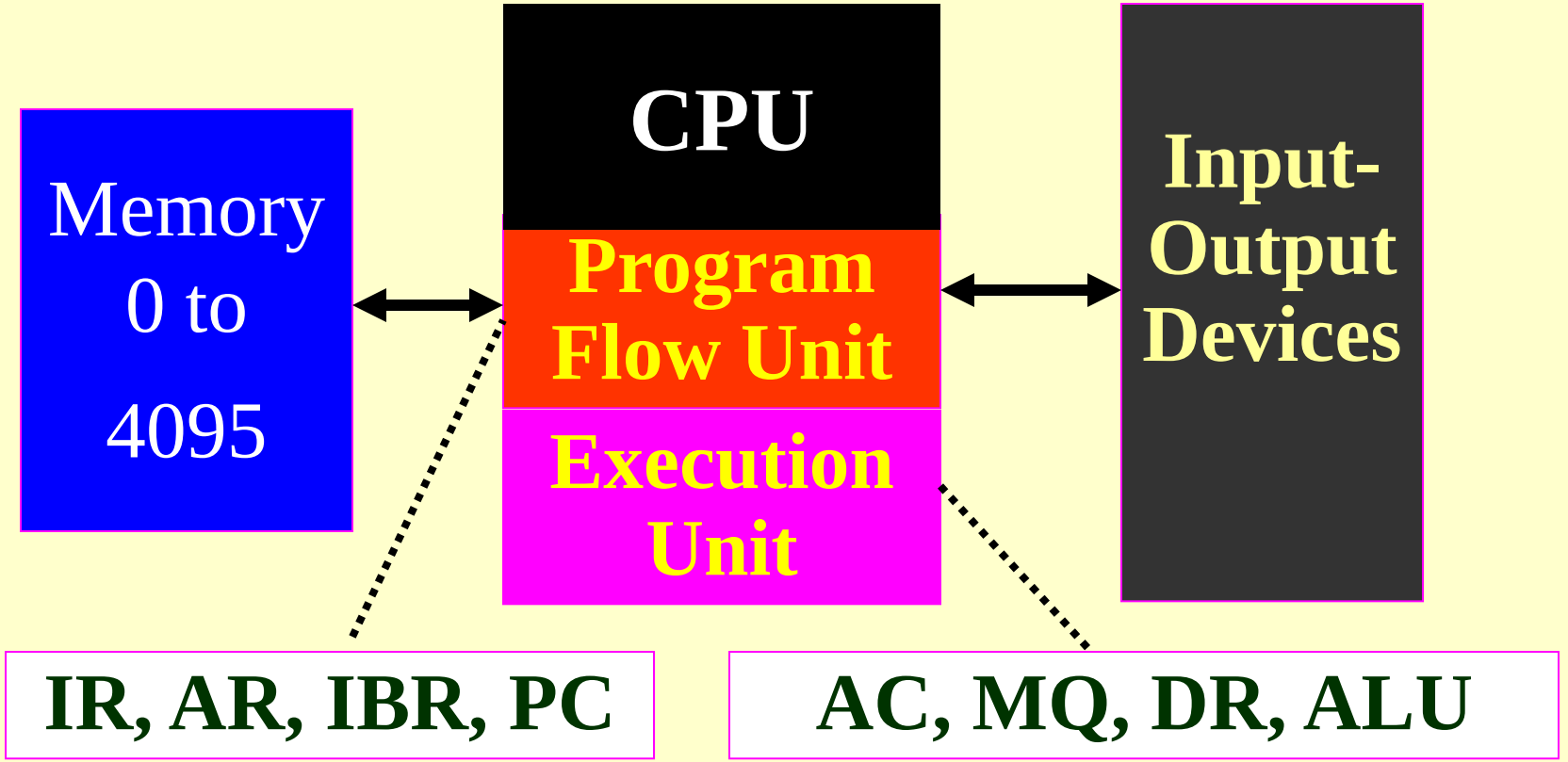
# IAS computer

- Hardware processed the data word by word and each word was stored as a 40-bit word
- Used 20-bit and 40-bit instruction format for the instructions

# IAS computer

- Introduced the instruction register (IR) concept
- IR held the instruction that had been fetched from the main memory
- Also held the next instruction in the cycle
- Used a program counter (PC) for address of instruction
- A cycle consisted of fetching and then execution of an instruction

# IAS (Institute of Advanced Studies) Princeton computer — Architecture



# IAS computer Architecture

- Instruction format –A2 OP
- A1 and A3 implicit in AC
- A4 implicit from PC
- Registers IR, AR, IBR, PC, AC, MQ, DR, ALU

# IAS computer Architecture

- CPU two units: program flow control (instructions flow) unit and execution unit.
- IR and AR (address register) the instruction and address registers
- Store the instruction from memory and for operand address, respectively

# IAS Architecture

- PC instruction address store for access to the main memory
- IBR the instruction buffer register,
- ALU the arithmetic and logic operations processing unit

# IAS Architecture

- DR the data register stored the data part of the instruction;
- AC the accumulator; and
- MQ a multiplier/quotient register

# Summary

## We learnt

- Tube-circuit-based computers— *first generation computers*
- 1st Generation of Computers 1943–1946 ENIAC
- EDVAC (Electronic Discrete Variable Automatic Computer) 1951
- IAS (Institute of Advanced Studies, Princeton) computer Architecture

## We learnt

- Stored computer concept
- Instruction format A1 A2 A3 A4 OP replaced by –A2 OP
- A1 and A3 implicit in AC
- A4 implicit from PC
- Registers IR, AR, IBR, PC, AC, MQ, DR, ALU

End of Lesson 01

**Evolution of Computers Part 2– First generation Computers**